ABSTRACT OF THE DISCLOSURE

Floating-gate memory cells having a trench source-line contact are suited for increased packing densities without a need for low-resistance ground straps placed at regular intervals across a memory array. Such floating-gate memory cells have their drain regions and source regions formed in a first semiconductor region having a first conductivity type. This first semiconductor region is separated from the underlying substrate by an interposing second semiconductor region having a second conductivity type different from the first conductivity type. The source regions of the memory cells are coupled to the second semiconductor region as a common source line. Such memory cells can be programmed, read and erased by applying various potential levels to their control gates, their drain regions, the first semiconductor region, and the second semiconductor region.